

## Claims

- [c1] A field effect transistor formed at a surface of a layer of semiconductor material, said field effect transistor comprising  
a gate structure formed on said surface of said layer of semiconductor material, and  
a discontinuous film of material within said layer of semiconductor material and having a discontinuity aligned with said gate structure.
- [c2] A field effect transistor as recited in claim 1, wherein said discontinuities are self-aligned with said gate structure.
- [c3] A field effect transistor as recited in claim 1, wherein said discontinuous film is a stressed film
- [c4] A field effect transistor as recited in claim 3, wherein said stressed film comprises an insulator.
- [c5] A field effect transistor as recited in claim 1, wherein said discontinuous film comprises an insulator.
- [c6] A field effect transistor as recited in claim 1, wherein said discontinuous film has a stepped or staircase profile

in cross-section.

- [c7] A field effect transistor as recited in claim 3, wherein said stressed film has a stepped or staircase profile in cross-section.
- [c8] A field effect transistor as recited in claim 7 wherein said stepped or staircase portion defines an effective channel depth.
- [c9] A field effect transistor as recited in claim 1, wherein said discontinuous film is an insulator including a portion formed of oxidized SiGe, wherein said discontinuity defines a location of a conductor connected to a channel of said field effect transistor.
- [c10] A field effect transistor as recited in claim 1, further including a void within said layer of semiconductor material.
- [c11] An integrated circuit including a field effect transistor formed at a surface of a layer of semiconductor material, said field effect transistor comprising a gate structure formed on said surface of said layer of semiconductor material, and a discontinuous film of material within said layer of semiconductor material and having a discontinuity aligned with said gate structure.

- [c12] An integrated circuit as recited in claim 11, wherein said discontinuous film has a stepped or staircase profile in cross-section.
- [c13] An integrated circuit as recited in claim 11 wherein said stepped or staircase portion defines an effective channel depth.
- [c14] An integrated circuit as recited in claim 11, wherein said discontinuous film is an insulator including a portion formed of oxidized SiGe, wherein said discontinuity defines a location of a conductor connected to a channel of said field effect transistor.
- [c15] An integrated circuit as recited in claim 11, further including a void within said layer of semiconductor material.
- [c16] A method of forming a hybrid field effect transistor or integrated circuit comprising steps of forming a gate structure, forming a discontinuous layer having a discontinuity aligned with said gate structure within a layer of semiconductor material underlying said gate structure.
- [c17] The method as recited in claim 8, wherein said gate structure is formed on a surface of said layer of semi-

conductor material.

[c18] A method as recited in claim 16, wherein said step of forming a discontinuous layer comprises steps of developing differential etch rates in respective portions of a continuous layer of semiconductor material, selectively etching a said portion of said continuous layer to form a void, and depositing material in said void.

[c19] A method as recited in claim 18, wherein said step of forming said discontinuous layer includes a step of oxidizing a surface of material exposed within said void.

[c20] A method as recited in claim 18, wherein said step of developing a differential etch rate includes a step of impurity implantation self-aligned with said gate structure.